IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: **CROCE ET AL.**	CERTIFICATE OF MAILING BY "EXPRESS MAIL" "EXPRESS MAIL" MAILING LABEL NUMBER EL769468485US DATE OF DEPOSIT April 20, 2001 I HEREBY CERTIFY THAT THIS PAPER OR FEE IS BEING DEPOSITED WITH THE UNITED STATES POSTAL SERVICE "EXPRESS MAIL POST OFFICE TO ADDRESSEE" SERVICE UNDER 37 CFR 1.10 ON THE DATE INDICATED ABOVE AND IS ADDRESSED TO THE COMMISSIONER OF PATENTS AND TRADEMARKS, WASHINGTON, D.C. 20231 Eric Link (TYPED OR PRINTED NAME OF PERSON MAILING PAPER OR FEE) (SIGNATURE OF PERSON MAILING PAPER OR FEE)
Serial No. **Not yet assigned**	
Filing Date: **Herewith**	
For: **RESURF LDMOS INTEGRATED STRUCTURE**	

PRELIMINARY AMENDMENT

Director, U.S. Patent and Trademark Office
Washington, D.C. 20231

Sir:

Prior to the calculation of fees and examination of the present application, please enter the amendments and remarks set out below.

In the Drawings:

Submitted herewith is a request for a proposed drawing modification as indicated in red ink to re-label FIG. 2 as FIGS. 2a and 2b and to label FIGS. 1a, 1b, and 2a as prior art. Furthermore, reference numbers are being added to FIGS. 1a, 1b, 2a, 2b, 3a, and 3b in accordance with the specification for clarity. Certain text is also being deleted from FIGS. 1a, 1b, 3a, and 3b for clarity. No new matter is being added.

In the Specification:

Please replace the paragraph beginning at page 2, line 18, with the following rewritten paragraph:

A typical shape of the depletion regions of the two above noted junctions is illustrated in FIG. 1a where the source 14, the body region **13**, and the gate are connected to a reference potential GND (i.e., Vg=Vsub=Vs=0) and a certain VDS voltage (e.g., VDS=20V) is applied to the drain. Under these operating conditions, the junctions are inversely biased because of the applied VDS voltage, and the respective depletion regions extend into the drain well region down to a certain depth. By further incrementing the VDS voltage, as shown in FIG. 1b (e.g., VDS=25V where Vg=Vsub=Vs=0), the depletion regions of the junctions between the substrate and the drain well region **12** and between the drain well region and the body region **13** merge. This completely depletes the drain well region **12**, thus producing the desired RESURF condition.

Please replace the paragraph beginning at page 4, line 16, with the following rewritten paragraphs:

FIG. 2a is a cross-sectional view illustrating a traditional LDMOS structure according to the prior art;

FIG. 2b is a cross-sectional view illustrating an LDMOS structure of the invention;

Please replace the paragraph beginning at page 5, line 24, with the following rewritten paragraph:

The principles upon which the RESURF LDMOS structure of the invention are based will be better understood with reference to FIGS. 3a and 3b. The BV measurements illustrated in FIG. 3a were obtained with Vds=70V and Vg=Vs=Vsub=0V, and the PT measurements illustrated in FIG. 3b were obtained with Vds=Vg=Vs=70V and Vsub=0V. As shown in FIG. 3b, even if

relatively high voltages are applied to the drain and source (typical of a high-side application), the drain well region **12** will be completely depleted of its charge before the body buffer region **15** is depleted. This is due to the heavier doping of the body buffer region **15**. This substantially prevents the occurrence of PT phenomena at relatively low voltages, which in turn enhances the performance of the structure of the invention under critical conditions of use.

In the Claims:

Please cancel Claims 1 to 4.

Please add new Claims 5 to 25.

5. A lateral diffused metal oxide semiconductor (LDMOS) integrated device comprising:

a semiconductor substrate;

a drain region of a first conductivity type adjacent said semiconductor substrate and comprising a superficial buffer region being more heavily doped than adjacent portions of said drain region;

a body region in said buffer region and having a second conductivity type; and

a source region in said body region and having the first conductivity type.

6. The LDMOS integrated device of Claim 5 wherein said drain region has a depth of about 1.5 to 4.5 micrometers.

7. The LDMOS integrated device of Claim 5 wherein the portions of said drain region adjacent said superficial buffer region have a dopant concentration of about $2.5x10^{15}$ to $2.5x10^{16}$ atoms cm^{-3}.

8. The LDMOS integrated device of Claim 5 wherein said superficial buffer region has a depth of about 0.15 to 0.45 micrometers.

9. The LDMOS integrated device of Claim 5 wherein said superficial buffer region has a dopant concentration of about $5x10^{16}$ to $5x10^{17}$ atoms cm^{-3}.

10. The LDMOS integrated device of Claim 5 wherein said body region has a depth of about 0.25 to 0.75 micrometers.

11. The LDMOS integrated device of Claim 5 wherein said body region has a dopant concentration of about $5x10^{17}$ to $5x10^{18}$ atoms cm^{-3}.

12. The LDMOS integrated device of Claim 5 wherein said drain region is doped with phosphorous; and wherein said body region is doped with boron.

13. The LDMOS integrated device of Claim 5 wherein said drain region is doped with boron; and wherein said body region is doped with phosphorus.

14. A lateral diffused metal oxide semiconductor (LDMOS) integrated device comprising:

a semiconductor substrate;

a drain region of a first conductivity type adjacent said semiconductor substrate and comprising a superficial buffer region being more heavily doped than adjacent portions of said drain region;

said superficial buffer region having a dopant concentration of about $5x10^{16}$ to $5x10^{17}$ atoms cm^{-3} and the adjacent portions of said drain region having a dopant concentration of about $2.5x10^{15}$ to $2.5x10^{16}$ atoms cm^{-3};

a body region in said superficial buffer region and having a second conductivity type; and

a source region in said body region and having the first conductivity type.

15. The LDMOS integrated device of Claim 14 wherein said drain region has a depth of about 1.5 to 4.5 micrometers.

16. The LDMOS integrated device of Claim 14 wherein said buffer region has a depth of about 0.15 to 0.45 micrometers.

17. The LDMOS integrated device of Claim 14 wherein said body region has a depth of about 0.25 to 0.75 micrometers.

18. The LDMOS integrated device of Claim 14 wherein said body region has a dopant concentration of about $5x10^{17}$ to $5x10^{18}$ atoms cm^{-3}.

19. A method for making a lateral diffused metal oxide semiconductor (LDMOS) integrated device comprising:

forming a drain region having a first conductivity type adjacent a semiconductor substrate;

forming a superficial buffer region having the first conductivity type in the drain region so that the buffer region is more heavily doped than adjacent portions of the drain region;

forming a body region having a second conductivity type in the superficial buffer region; and

forming a source region having the first conductivity type in the body region.

20. The method of Claim 19 wherein the drain region has a depth of about 1.5 to 4.5 micrometers.

21. The method of Claim 19 wherein the portions of the drain region adjacent said superficial buffer region have a dopant concentration of about $2.5x10^{15}$ to $2.5x10^{16}$ atoms cm^{-3}.

22. The method of Claim 19 wherein the superficial buffer region has a depth of about 0.15 to 0.45 micrometers.

23. The method of Claim 19 wherein the superficial buffer region has a dopant concentration of about $5x10^{16}$ to $5x10^{17}$ atoms cm^{-3}.

24. The method of Claim 19 wherein the body region has a depth of about 0.25 to 0.75 micrometers.

25. The method of Claim 19 wherein the body region has a dopant concentration of about $5x10^{17}$ to $5x10^{18}$ atoms cm^{-3}.

REMARKS

Attached hereto is a marked-up version of the changes made to the specification by the current amendment. The attached pages are captioned **"Version With Markings to Show Changes Made."**

It is believed that all of the claims are patentable over the prior art. For better readability and the Examiner's convenience, the newly submitted claims differ from the translated counterpart claims which are being canceled. The newly submitted claims do not represent changes or amendments that narrow the claim scope for any reason related to the statutory requirements for patentability.

Accordingly, after the Examiner completes a thorough examination and finds the claims patentable, a Notice of Allowance is respectfully requested in due course. Should the Examiner determine any minor informalities that need to be addressed, he is encouraged to contact the undersigned attorney at the telephone number below.

In re Patent Application of
CROCE ET AL.
Serial No. **Not Yet Assigned**
Filed: **Herewith**

Respectfully submitted,

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In re Patent Application of
CROCE ET AL.
Serial No. **Not Yet Assigned**
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_____/

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Specification:

Paragraph beginning at page 2, line 18 has been amended as follows:

A typical shape of the depletion regions of the two above noted junctions is illustrated in FIG. 1a where the source 14, the body region **13**, and the gate are connected to a reference potential GND (i.e., Vg=Vsub=Vs=0) and a certain VDS voltage (e.g., VDS=20V) is applied to the drain. Under these operating conditions, the junctions are inversely biased because of the applied VDS voltage, and the respective depletion regions extend into the drain well region down to a certain depth. By further incrementing the VDS voltage, as shown in FIG. 1b (e.g., VDS=25V where Vg=Vsub=Vs=0), the depletion regions of the junctions between the substrate and the drain well region **12** and between the drain well region and the body region **13** merge. This completely depletes the drain well region **12**, thus producing the desired RESURF condition.

Paragraph beginning at page 4, line 16 has been amended as follows:

FIG. 2a is a cross-sectional view illustrating a traditional LDMOS structure according to the prior art; [and a]

FIG. 2b is a cross-sectional view illustrating an LDMOS structure of the invention;

Paragraph beginning at page 5, line 24 has been amended as follows:

The principles upon which the RESURF LDMOS structure of the invention are based will be better understood with reference to FIGS. 3a and 3b. The BV measurements illustrated in FIG. 3a were obtained with Vds=70V and Vg=Vs=Vsub=0V, and the PT measurements illustrated in FIG. 3b were obtained with Vds=Vg=Vs=70V and Vsub=0V. As shown in FIG. 3b, even if relatively high voltages are applied to the drain and source (typical of a high-side application), the drain well region **12** will be completely depleted of its charge before the body buffer region **15** is depleted. This is due to the heavier doping of the body buffer region **15**. This substantially prevents the occurrence of PT phenomena at relatively low voltages, which in turn enhances the performance of the structure of the invention under critical conditions of use.

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SUBMISSION OF PROPOSED MODIFICATIONS TO DRAWINGS

Director, U.S. Patent and Trademark Office
Washington, D.C. 20231

Sir:

Submitted herewith is a request for a proposed drawing modification as indicated in red ink to re-label FIG. 2 as FIGS. 2a and 2b and to label FIGS. 1a, 1b, and 2a as prior art. Furthermore, reference numbers are being added to FIGS. 1a, 1b, 2a, 2b, 3a, and 3b in accordance with the specification for clarity. Certain text is also being deleted from FIGS. 1a, 1b, 3a, and 3b for clarity. No new matter is being added.

Respectfully submitted,

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Eric Link
(TYPED OR PRINTED NAME OF PERSON MAILING PAPER OR FEE)

(SIGNATURE OF PERSON MAILING PAPER OR FEE)

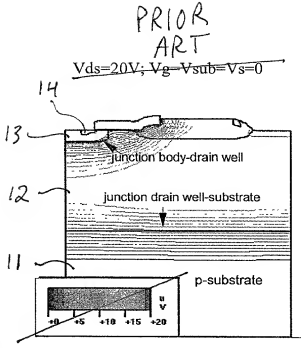

Fig. 1a

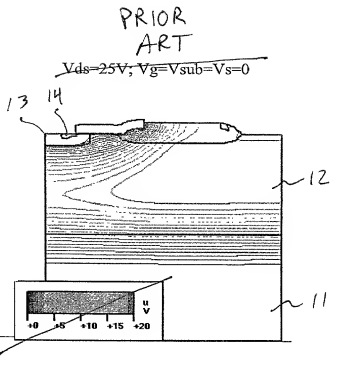

Fig. 1b

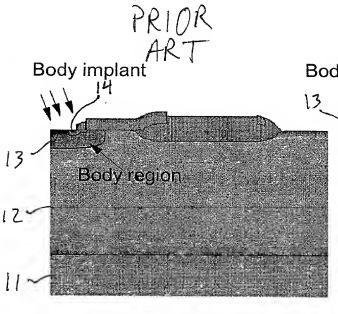

Fig. 2a

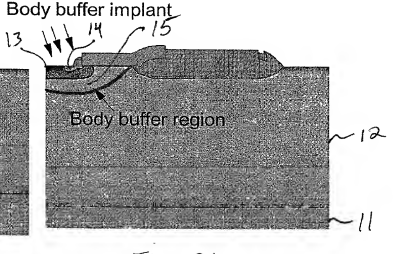

Fig. 2b

Fig. 2

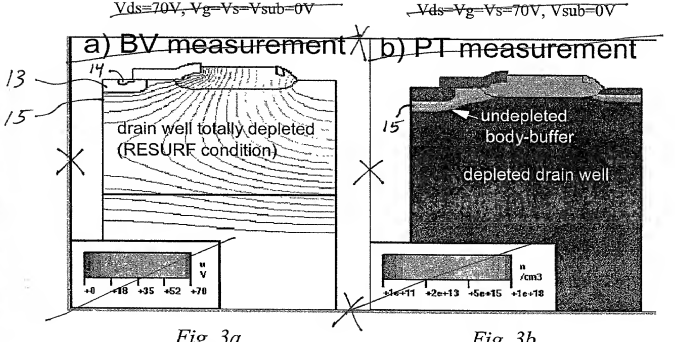
Vds=70V, Vg=Vs=Vsub=0V
a) BV measurement
13
14
15
drain well totally depleted
(RESURF condition)
+0
+18
+35
+52
+70
Vds=Vg=Vs=70V, Vsub=0V
b) PT measurement
15
undepleted
body-buffer
depleted drain well
+1e+11
+2e+13
+5e+15
+1e+18
/cm3

Fig. 3a *Fig. 3b*